Configurable Digital Pulse Generator for Neuromorphic Devices

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***Abstract*—In this paper, we propose a configurable pulse generator for neuromorphic devices to verify the resistance change characteristics of neuromorphic devices. In general, the resistance change characteristics of neuromorphic devices are verified based on both the number of pulses and pulse width. The proposed configurable digital pulse generator consists of two sub-modules: Pulse Width Controller (PWC) that determines the pulse width and Pulse Count Controller (PCC) that specifies the number of pulses. Due to the configurable property, the proposed pulse generator can be widely applied to the various environment to verify the neuromorphic devices. As an experiment, The digital pulse generator was designed using a CMOS 180nm process, and it was shown that it can be used to verify the resistance change characteristics of neuromorphic devices through operation verification.**

Keywords— neuromorphic device; configurable; digital; pulse generator

I. INTRODUCTION

In the recent years, AI technology has been explosively used in various applications. In contrast to the active development of algorithms and architecture software for continuous improvement of AI performance, the speed and energy efficiency of hardware processing AI are rapidly reaching theoretical limits [1]. The neuromorphic architecture, which mimics the process of learning and computing by the human brain, is expected to perform 3,000 times faster deep learning operation than the existing CPU/GPU [2] and the advantage of ultra-low power due to the parallel processing structure. It is emerging as an alternative to traditional computer architecture.

Neuromorphic architecture is usually constructed in an array form using neuron devices and synaptic devices as shown in Figure 1 [3,4]. Neuron devices have the characteristic of transmitting information when the accumulated input spike value reaches a specific threshold [5,6]. Synapse devices represent the strength of connections between neurons, and have the characteristic of learning the strength of connections by input spikes [7,8]. Since both devices have different resistance change characteristics depending on the circuit structure and input spikes, it is essential to verify the characteristics of resistance change for the development of neuromorphic devices [5-8].

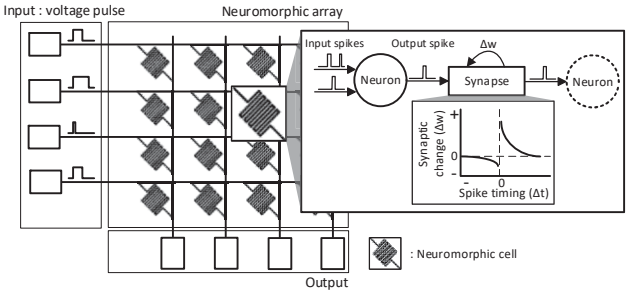


Fig. 1. Typical neuromorphic device verification method.

Most of the characteristics of neuromorphic devices are tested in a popular form of controlled pulses. In general, it is test for the multiple times by adjusting pulse width, number of pulses, and magnitude of pulse voltage [5-8]. In this paper, we propose a configurable digital pulse generator for neuromorphic devices to measure the change in resistance characteristics of neuromorphic devices repeatedly. Through verification of the operation of the digital pulse generator, it is shown that the change in resistance characteristics of neuromorphic devices can be measured [5-8].

II. PROPOSED DIGITA PULSE GENERATOR

As shown in Fig. 2, the proposed configurable digital pulse generator consists of Pulse Width Controller (PWC) that controls pulse width and Pulse Count Controller (PCC) that control number of pulses.

Firstly, PWC consist of a counter and a multiplexer (MUX) to controls the pulse width. It is designed to be controlled to the desired pulse width using an output corresponding to each bit of the counter and a multiplexer that outputs one of several input signals based on the control signal. Since the counter increments by one every clock cycle, the output of counter in bits provide different toggle period. More precisely, the toggle period of pwc_cnt[i+1] is two times slower than the toggle period of pwc_cnt [i]. Thus, the output of the counter is used to generate different width of pulses. When applying 7-bit counter, the minimum pulse width is the same as the clock period, and the maximum pulse width is 128 times slower than the clock

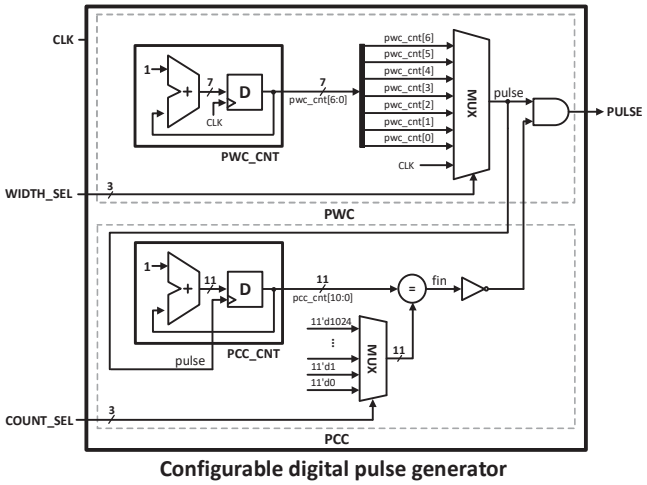


Fig. 2. The proposed configurable digital pulse generator.

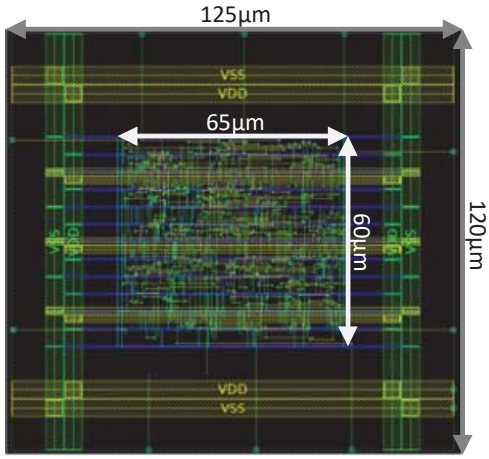


Fig. 3. Chip Layout of the proposed configurable digital pulse generator.

period. As an example, the minimum configurable pulse width is 4ns and the maximum configurable pulse width is 512ns when an operating frequency is of 250MHz.

Similar to PWC, PCC consists of a counter and a MUX to control the number of pulses. Once a width-configured-pulse is generated by PWC, PCC generates such pulse as many as the configured number. The counter in PCC counts the number of width-configured-pulses, and it terminates the operation when it reaches the desirable number by comparing the number of selected pulses and the output bits of the counter. It is important to note that the clock for the counter in PCC is the output of PCC to generate width-configured-pulses as many as the configured number.

As shown in Fig. 2, the configurable digital pulse generator consists of two modules PWC and PCC connected, and the desired pulse width and the number of pulses can be generated according to the control signal applied to each sub-module. As a result, configurable digital pulse generator can verify the resistance change characteristics of the neuromorphic devices by adjusting pulse width and number of pulses [5-8].

III. IMPLEMENATION RESULTS

To verify the proposed digital pulse generator, it is synthesized and implemented with 250MHz operating frequency using CMOS 180nm process. PWC is designed to adjust the pulse width from minimum 4ns to maximum 512ns by setting the operating frequency as 250MHz, and PCC is designed to control the number of pulses from a minimum of 0 to a maximum of 1024 by setting the counter in PCC to 11 bits. Table 1 summarizes the synthesis results. The digital pulse generator demands 0.015mm^2 for equivalent gate count of 303, and it can provide throughput up to 298.50 Mbps with the critical path delay of 3.35 ns. For CMOS 180nm process used in the implementation, The metal layer is supported up to 6 layers, but the proposed design is synthesized and implemented with the limited metal layer up to 3 for the future integration with neuromorphic devices. In order to verify the operation of the configurable digital pulse generator, clock and control signals are applied to the implemented chip, and it is checked whether it operates normally through the generated output.

TABLE I. IMPLEMENTATION RESULTS

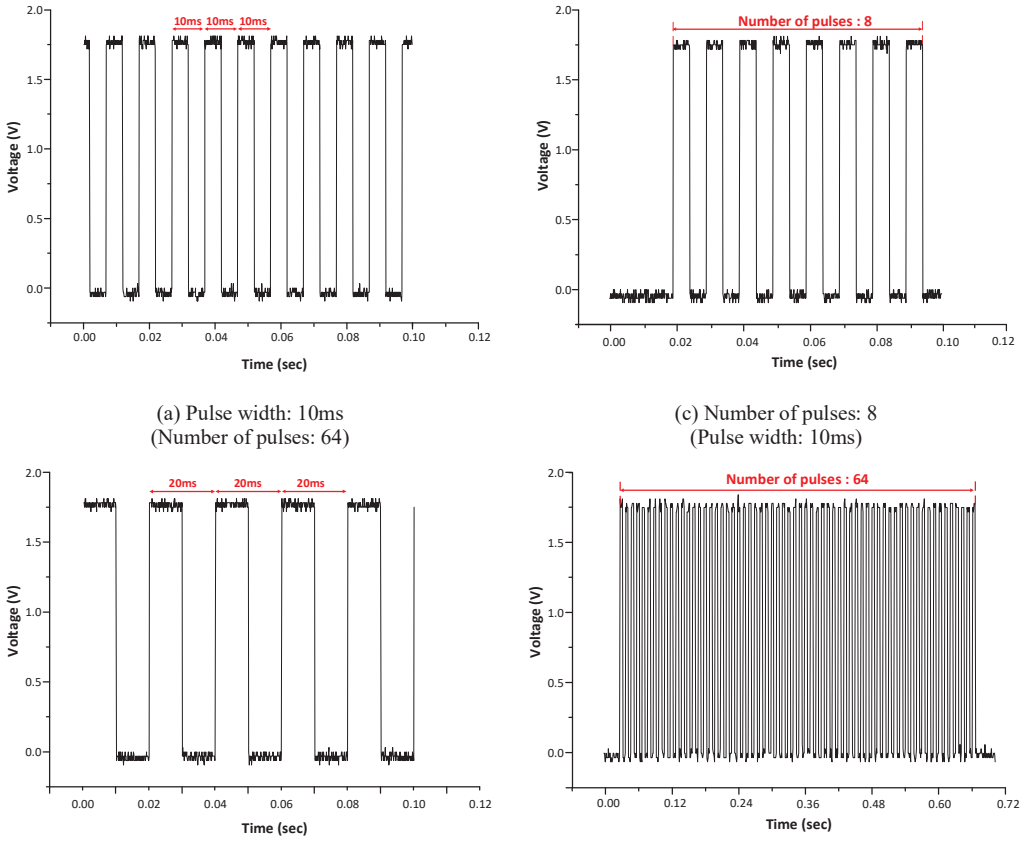
Physical Metrics	Digital pulse generator
Area	0.015mm^2 (125µm x 120µm)
Equivalent Gate Count	303
Critical-Path Delay	3.35 ns
Throughput	298.50 Mbps
Max Metal Layer	3

The output pulse was verified by using an oscilloscope with a sampling rate of 4GSa/s.

To test configurability of the proposed digital pulse generator, different control signals are applied. Fig. 4 shows that the proposed digital pulse generator can provide configurable width and numbers according to the control signals. Fig. 4(a) and Fig. 4(b) describes the generated pulses with the period of 10ms and 20ms, respectively. The counter in PWC can control the width of pulses in the proposed digital pulse generator. In addition, Fig. 4(c) and Fig. 4(d) describes the generated pulses with the number of 8 and 64, respectively. The counter in PCC can control the number of pulses in the proposed digital pulse generator.

IV. CONCLUSION

In this paper, configurable digital pulse generator for neuromorphic devices is proposed to verify the resistance change characteristics of neuromorphic devices. The proposed digital pulse generator with internal sub-modules PWC and PCC can generate various pulses with different width and numbers. Through operation verification based on silicon chip, it was shown that the proposed digital pulse generator can improve test productivity to verify the characteristics of neuromorphic devices [5-8]. In the future, digital pulse generators are expected to be able to verify more precise resistance change characteristics compared to conventional measuring devices by integrating with neuromorphic architecture [5-8] in a single chip.



(a) Pulse width: 10ms
(Number of pulses: 64)

(c) Number of pulses: 8
(Pulse width: 10ms)

(b) Pulse width: 20ms
(Number of pulses: 64)

(d) Number of pulses: 64
(Pulse width: 10ms)

Fig. 4. Experimental result for various pulse width and number of pulses.

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